PRESENTATION OUTLINE

I. CALCULATOR CHIPS HISTORY

- A. REGISTER PROCESSORS
- B. DIGIT PROCESSORS

II. LCD III

- A. DESIGNATIONS
- B. DESIGN GOALS / METHODS
- C. LCD III BLOCK DIAGRAM
- D. SYSTEM CONFIGURATION POSSIBILITIES

III. PRODUCT X

- A. GOALS / FEATURES
- B. BLOCK DIAGRAM
- C. SCHEMATIC
- D. I/O

COMMON FEATURES OF CALCULATOR CHIPS

- SINGLE CHIP MICROCOMPUTER
  - ON BOARD ROM
  - ON BOARD RAM
  - INTEGRATED I/O DECODING AND BUFFERING
- SIMPLE ALU
  - USUALLY BINARY ADDITION, NEGATION, AND COMPARE AVAILABLE
  - CALCULATIONS ARE CONVERTED TO DECIMAL BY SOFTWARE
- LARGE ROM
  - USUALLY DIVIDED INTO PAGES
  - USUALLY NOT EXPANDABLE
- RAM
  - USUALLY ORGANIZED AS 64 BIT REGISTERS
  - USUALLY NOT EXPANDABLE
- PROGRAM COUNTER
  - USUALLY A SHIFT COUNTER
  - COUNTS IN ODD SEQUENCE
  - MAKES IT VERY DIFFICULT TO USE INDIRECT OR RELATIVE ADDRESSING
- ALL OF THE FEATURES ABOVE REQUIRE THE MINIMUM SILICON AREA ON THE CHIP AND CONTRIBUTE TO LOW COST

CALCULATOR ARCHITECTURES

SPLIT ARCHITECTURE

- SEPARATE MEMORY AREAS FOR PROGRAM STORAGE AND DATA MEMORY
- SEPARATE ADDRESSING SCHEMES AND DIFFERENT BIT LENGTHS FOR THE TWO MEMORY TYPES

REGISTER PROCESSORS

- OPERATIONS ARE DONE ON ENTIRE REGISTERS
  - USUALLY 64 BIT REGISTERS (16 DIGITS x 4 BITS)
    INSTRUCTIONS SPECIFY ONE OF SEVERAL AVAILABLE "MASKS" TO OPERATE ON PORTIONS OF THE REGISTER: MANTISSA, EXPONENT, OR ALL
  - OPERATIONS INCLUDE DECIMAL ADDITION WITH AUTOMATIC CARRY BETWEEN DIGITS
- NO POINTER SYSTEM FOR DATA ADDRESSING
  - THE INSTRUCTION SPECIFIES WHICH REGISTERS
  - ADDRESSING INDIVIDUAL DIGITS IS NOT POSSIBLE
- INSTRUCTION CYCLES ARE TYPICALLY 80-100 μSEC
- EXCELLENT FOR FAST ARITHMETIC CALCULATIONS
- NOT FLEXIBLE ENOUGH FOR SPECIALTY PRODUCTS SINCE DIGIT MANIPULATION IS NOT POSSIBLE
- EXAMPLES: TMC0500, TMC1500, TMC0920, TP0310, (SEE FIGURE 1)

DIGIT PROCESSORS

- OPERATIONS ARE DONE ON 4 BIT DIGITS
  - A 4 BIT BINARY ADDER AND 4 BIT ACCUMULATOR (TEMPORARY HOLDING REGISTER) ARE THE BASIC TOOLS

- A POINTER SYSTEM LOCATES THE 4 BIT PIECE OF DATA TO BE OPERATED ON
  - ONE POINTER SELECTS ONE OF THE REGISTERS
  - ONE POINTER SELECTS ONE DIGIT IN THAT REGISTER

- INSTRUCTION CYCLES ARE TYPICALLY 15-30 μSEC

- EXECUTION OF ARITHMETIC CALCULATIONS IS TYPICALLY SLOWER THAN REGISTER PROCESSORS SINCE THESE CALCULATIONS REQUIRE A SUBROUTINE INSTEAD OF A SINGLE INSTRUCTION
  - SOME DIGIT PROCESSORS SUCH AS LCDIII HAVE SPECIAL FEATURES WHICH ALLOW ARITHMETIC CALCULATIONS AT REGISTER PROCESSOR SPEED

- EXTREMEMLY FLEXIBLE
  - EFFECTIVE REGISTER SIZE, NUMBER OF FLAGS, AND I/O ARE ALL CONTROLLED BY SOFTWARE
  - USEFUL AS CONTROLLERS AND FOR PROCESSING ODD DATA STRUCTURES (PRINTERS, SPECIALTY PRODUCTS)

- EXAMPLES: TMC1000, TMC0980, TMC1980, TMC0260, TMC0270, TP0320, TP0455, LCDIII (TP0475, TP0480) (SEE FIGURE 2)

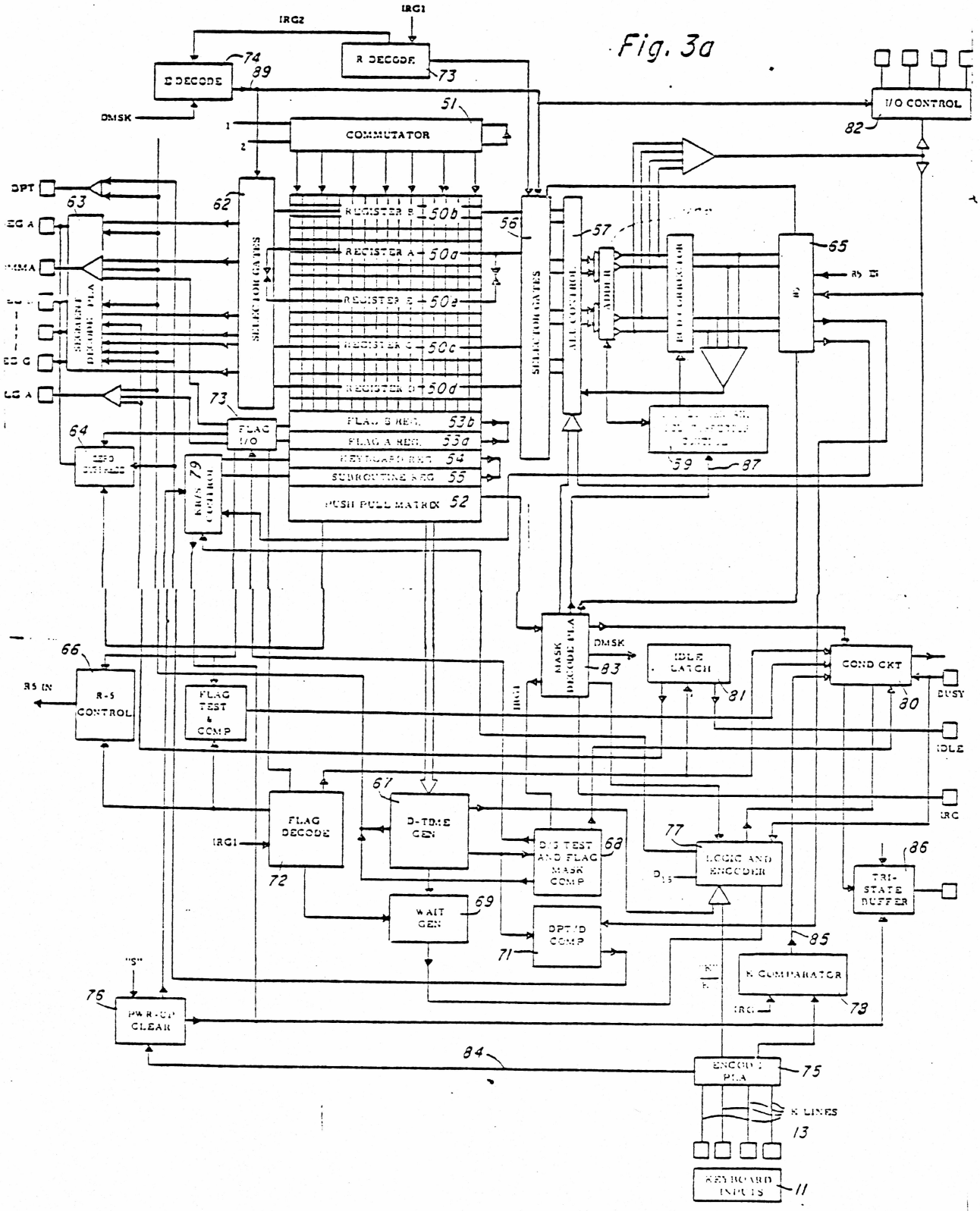
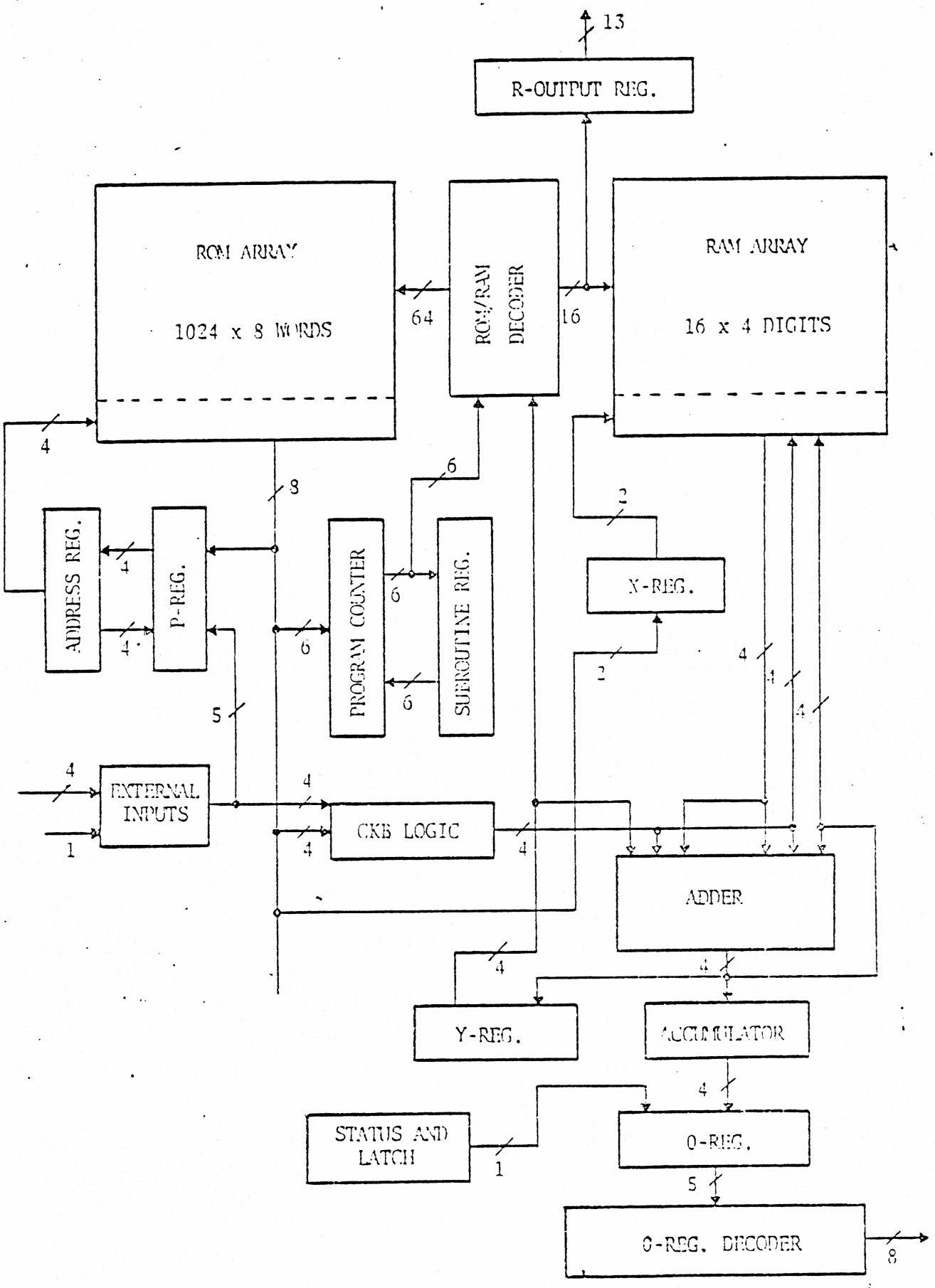


Fig. 3a

TMC0500

FIGURE 1



TMC1000

FIGURE 2

CHIP DESIGNATIONS

OLD DESIGNATIONS

A = 1K ROM

B = 2K ROM

C = 3K ROM

F = FAST ROM
T = TIMEKEEPING

C22FT = 3K ROM, 22x16x4 bit RAM Registers, Fast ROM, and Timekeeping

NEW DESIGNATIONS

TP 0480 = C22FT WITH LCD DRIVE (TI 55)

TP 0475 = C22FT WITHOUT LCD DRIVE (PRODUCT X) SOMETIMES CALLED "PXT"

TP 0470 = C22F WITHOUT LCD DRIVE (PRODUCT X) SOMETIMES CALLED "PX"

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COMPONENT DESIGN
LCD III STATUS REVIEW

MAJOR SYSTEM GOALS

- CONVERT CALCULATOR PRODUCTS FROM BASIC CONSUMER THROUGH TI-57 TO LONG BATTERY LIFE, LC DISPLAYS
- PROVIDE THE BASIS FOR A HIGH PERFORMANCE TI-59 REPLACEMENT
- AFFORD THE FLEXIBILITY TO PRODUCE NEW, NON-CALCULATOR CONSUMER PRODUCTS, INCLUDING COMPLEX TIMEKEEPING FUNCTIONS
- NON VOLATILE PROGRAM AND DATA STORAGE FOR MOST CALCULATOR MODELS
- LOW UNIT COST/FUNCTION
- LONG DESIGN SERVICE LIFE

COMPONENT DESIGN

LCD III STATUS REVIEW

APPROACH

MODULAR DESIGN

LAYOUT: EACH PROCESSOR IS A SUBSET OF THE NEXT LARGER CIRCUIT. LITTLE OR NO LAYOUT WORK IS REQUIRED TO GENERATE THE CORES OF THE SMALLER VERSIONS OF THE SYSTEM.

CELL DESIGN: WHEREVER POSSIBLE, CELLS WITH SIMILAR FUNCTIONS WILL BE DESIGNED AS IDENTICAL UNITS.

ARCHITECTURE: I/O AND SPECIAL FUNCTIONS ARE TREATED AS MEMORY LOCATIONS TO ELIMINATE SPECIAL INSTRUCTIONS. ROM AND RAM ADDRESSING IS PAGED TO PERMIT EASY EXPANSION WITH MINIMAL BURDEN ON SMALLER VERSIONS.

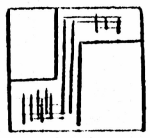
COMPONENT DESIGN
LCD III STATUS REVIEW

APPROACH RATIONALE

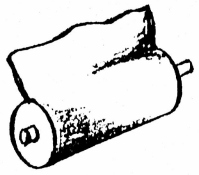
- DEVELOPMENT OF SEVERAL CHIPS FROM ONE DESIGN REDUCES MONEY, TIME AND MANPOWER REQUIREMENTS
- MODULAR DESIGN GREATLY REDUCES DEVELOPMENT TIME AND COST FOR FUTURE CUSTOM PROCESSOR REQUIREMENTS
- COMMON INSTRUCTION SET REDUCES ALGORITHM DEVELOPMENT TIME BY UTILIZING PROGRAMMER LEARNING AND PREVIOUSLY DESIGNED ROUTINES

PROCESSOR APPLICABILITY

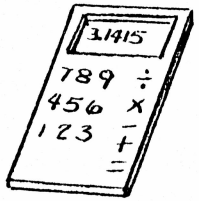
LCD III



"A" CHIP



PRINTER DRIVE

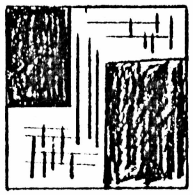


FOUR FUNCTION

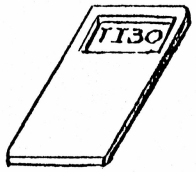
PRODUCT X I/O CONTROL

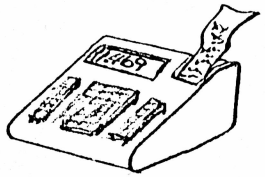
0500

NONE

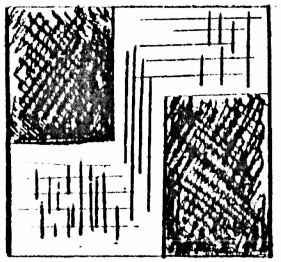


"B" CHIP





NONE



"C" CHIP

TI-55

PRODUCT X CONTROLLER

PRODUCT X NUMBER CRUNCHER

501
580

05-26-78 AH 039-639

COMPONENT DESIGN
LCD III STATUS REVIEW

APPLICATIONS

PRODUCT TYPE	LCD III VERSION
TI 1000, 1025	A
LITTLE PROFESSOR	A
DATAMAN	B
CALCULATOR/CLOCK	B + TIME
EXECUTIVE REMINDER	(2) B OR B + C
TRAVEL ALARM	B + TIME, EXT RAM
TI-30, BUSINESS ANALYST	B
TI-55, 57	C
PRODUCT X CONTROLLER	C

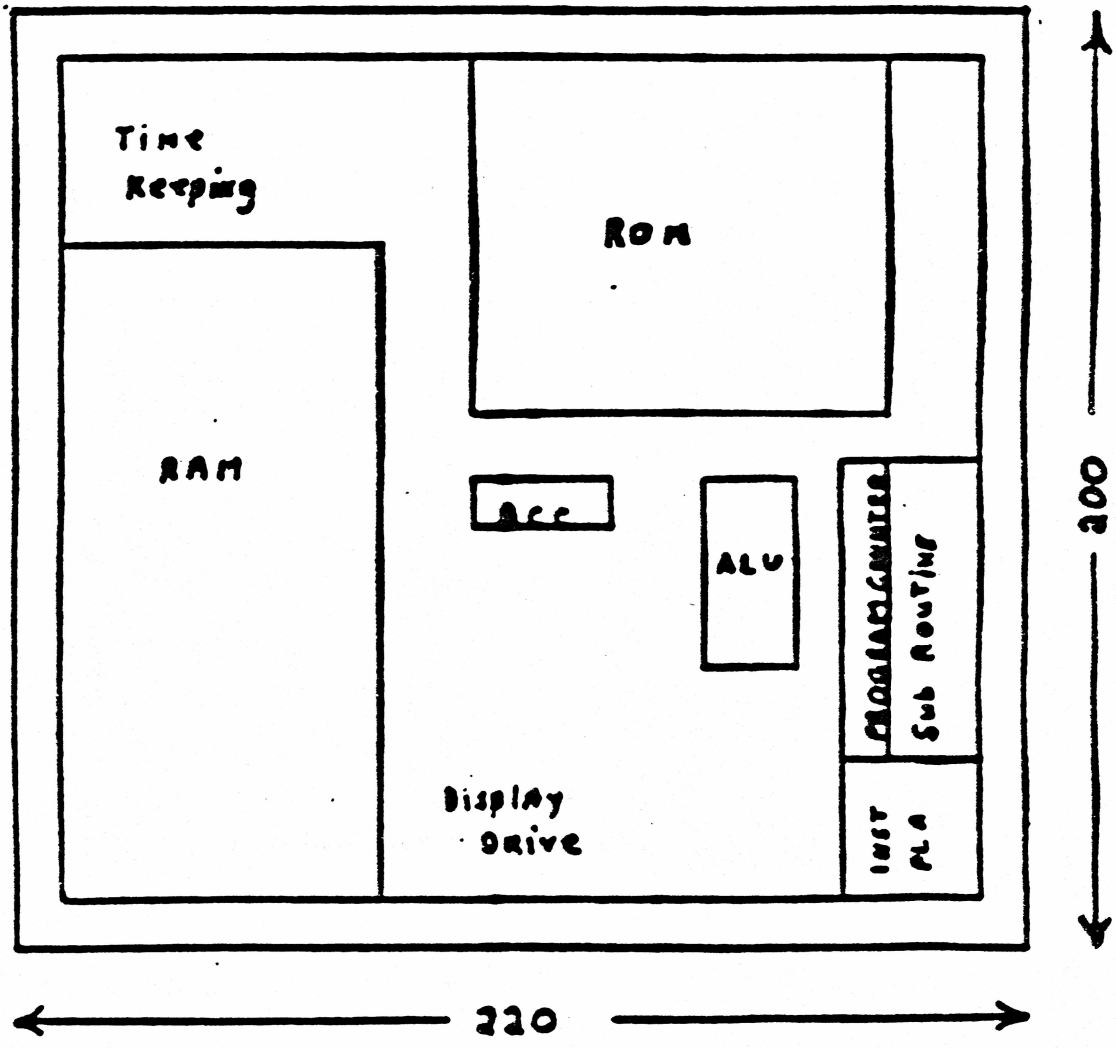
IN GENERAL,

CHIP A REPLACES TMC 1000, TMC 0970, TMC 1990, TMC 0920
TP 0310

CHIP B REPLACES TMC 0980, TMC 1980, TMC 1100, TP 0320

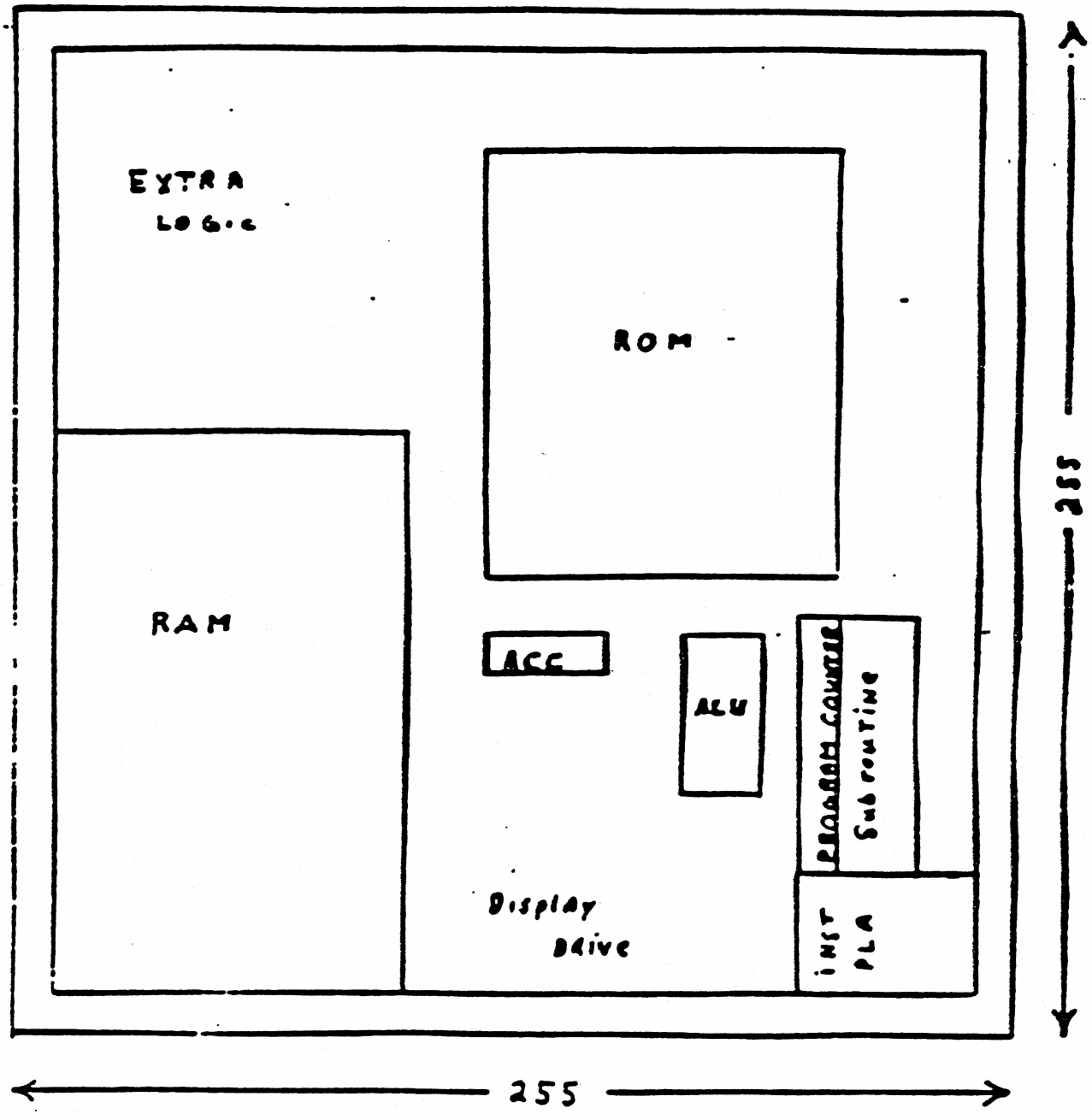
CHIP C REPLACES TMC 1500

EACH VERSION IS MORE POWERFUL THAN THE CIRCUITS IT REPLACES



CHIP B

GRABER.



CHIP C

GRARCO

COMPONENT DESIGN
ADVANCED SOFTWARE DEVELOPMENT

LCD III
FEATURES OF LCD III APPROACH

- EFFICIENT
- FLEXIBLE
- REDUCED PACKING PROBLEMS
- MODULAR OR REUSABLE SOFTWARE
- SOFTWARE COMPABILITY AMONG CHIP SETS

MAY OPERATIONS REVIEW
COMPONENT DESIGN

LCD III PERFORMANCE GOALS

- EFFICIENCY OF A DIGIT PROCESSOR
  - WELL STRUCTURED LOGIC ARRAYS WITH TIGHT DESIGN RULES MINIMIZE BAR AREA
  - BIT/BYTE DATA ACCESS
  - SOFTWARE DEFINABLE I/O BUS STRUCTURES
- SPEED OF A REGISTER PROCESSOR
  - ONE CYCLE REGISTER ARITHMETIC
  - DIRECT MEMORY ADDRESSING

MAY OPERATIONS REVIEW
COMPONENT DESIGN

EXECUTION SPEED

LCD III DESIGN APPROACH: TO ACHIEVE FAST EXECUTION TIMES WITH A DIGIT PROCESSOR

FAST ROM

- 128 x 13 BITS - SMALL SIZE ALLOWS FASTER ROM ACCESS
- BASIC ADD AND SHIFT LOOPS ARE PLACED IN FAST ROM
- REDUCES MULTIPLY TIMES BY 50%

DUAL REGISTER POINTER SYSTEM

- EACH OPERAND IN AN ADDITION HAS A SEPARATE POINTER
- NO WASTED TIME MOVING SINGLE POINTER BETWEEN TWO REGISTERS

HOLD PROGRAM COUNTER

- ONE INSTRUCTION LOOP

MAY OPERATIONS REVIEW
COMPONENT DESIGN
SPEED COMPARISONS

		LCD III	TMC 0500
INSTRUCTION CYCLE		15 μ SEC	83 μ SEC
	FAST ROM =	5 μ SEC	
MULTIPLY SUBROUTINE		30 MSEC	27 MSEC
FLAG TEST		30 μ SEC	155 μ SEC

MEMORY ACCESS	STANDARD RAM	PC RAM	
PROGRAM STEP	0.65 MSEC	0.18 MSEC	0.5 MSEC
USER MEMORY	6.2 MSEC	4.1 MSEC	1.5 MSEC
ABSOLUTE GOTO	3.6 MSEC	0.55 MSEC	36.0 MSEC

MAY OPERATIONS REVIEW
COMPONENT DESIGN

INSTRUCTION SET CAPABILITIES

	LCD III	TMC 0500	TMC 0980
• DIRECT MEMORY ADDRESSING	FLAGS, BYTES	FLAGS, REGISTERS	NO
• MEMORY MAPPED I/O	YES	NO	NO
• LOGIC INSTRUCTIONS	YES	NO	LIMITED
• INDIRECT ROM ADDRESSING	PC INDEXING	YES	NO
• INDIRECT RAM ADDRESSING	YES	NO	LIMITED
• ROM PAGING	1K	1K	128
• CONDITIONAL BRANCHING	SET, RESET	SET, RESET	SET ONLY
• SUBROUTINE LEVELS	6	1-LIMITED	1

COMPONENT DESIGN
ADVANCED SOFTWARE DEVELOPMENT

LCD III INSTRUCTION SET
TEST RESULTS
EFFICIENCY

TEST PROGRAM	CAL. CHIP	LCD III	PERFORMANCE
1. MULTIPLICATION	TI30 939		
	117 INS.	105 INS.	10.2% DECREASE
2. E^X	TI55 1500		
	240 INS.	307 INS.	27.9% INCREASE
3. PROGRAMMING (LRN)	TI 55 1500		
	63 INS.	57 INS.	9.5% DECREASE
4. PROGRAMMING (LRN)	TI57 1500		
	116 INS.	125 INS.	7.7% INCREASE

COMPONENT DESIGN
ADVANCED SOFTWARE DEVELOPMENT

FLEXIBILITY

- SPEED OF A REGISTER PROCESSOR WITH FLEXIBILITY OF DIGIT PROCESSOR.
- INPUT/OUTPUT IS ALL UNDER SOFTWARE CONTROL AND "MEMORY MAPPED" FOR FLEXIBILITY.
- RAM MAY BE SUBDIVIDED AS DESIRED WITH SOFTWARE
- MICROPROCESSOR APPLICATIONS CAN BE HANDLED AS EASILY AS REGISTER OPERATIONS.

COMPONENT DESIGN
ADVANCED SOFTWARE DEVELOPMENT

PACKING PROBLEMS

- DUE TO LARGE 1K WORD ROM PAGES THE PROBLEMS OF PACKING ACROSS PAGE BOUNDARIES ARE LARGELY AVOIDED.

MODULAR SOFTWARE

- LARGE ROM PAGES MEAN SOME STANDARD ROUTINES MAY BE REMOVED FROM ONE ALGORITHM AND FIT TOGETHER INTO OTHERS RATHER EASILY.

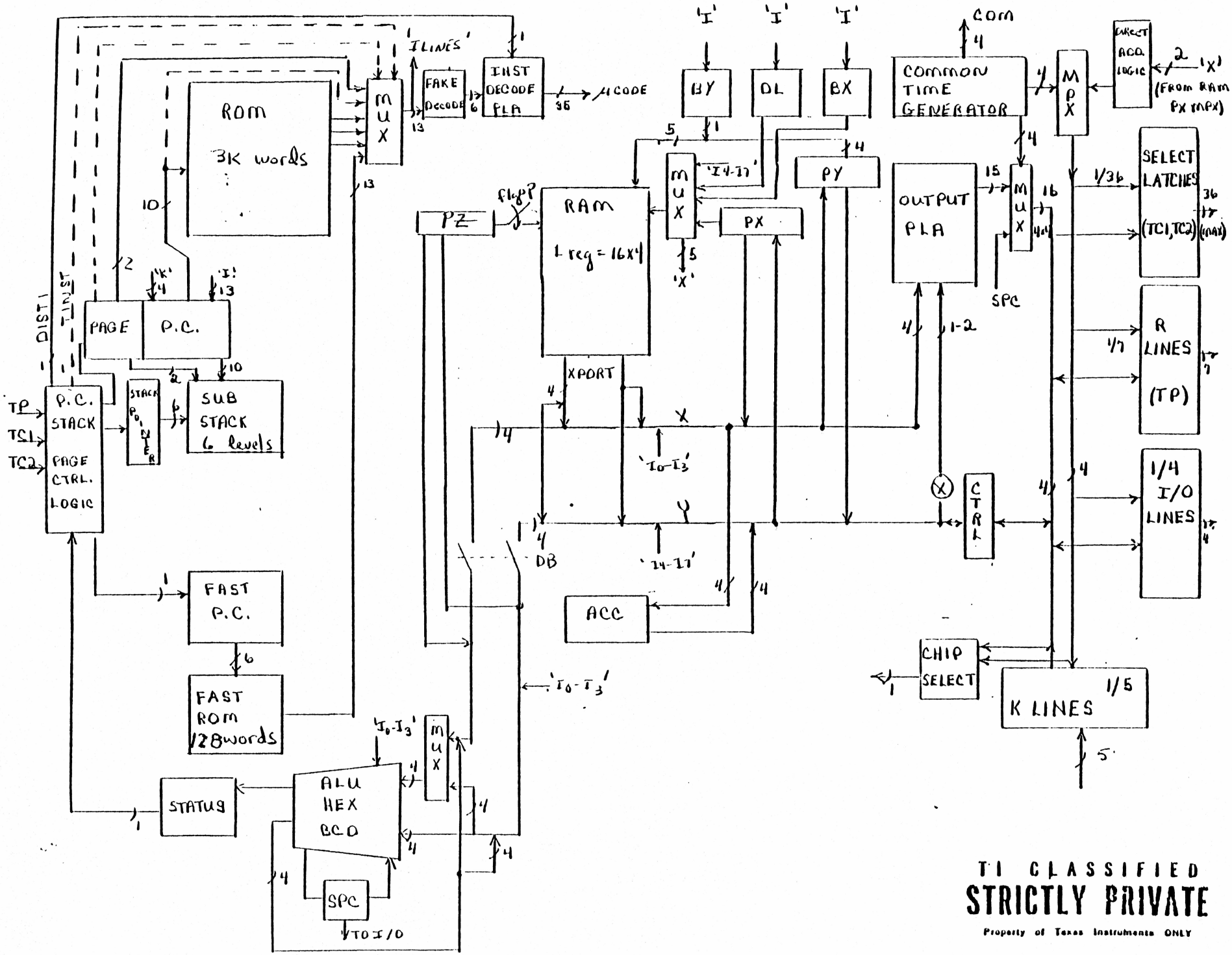
SOFTWARE COMPATIBILITY

- ALL CHIPS IN THIS FAMILY USE THE SAME INSTRUCTION SET.
- PROGRAMMERS EXPERIENCED ON ONE CHIP ARE EXPERIENCED ON ENTIRE FAMILY.
- ALGORITHM FROM ONE CHIP MAY BE USED ON ANY OTHER CHIP IN THE FAMILY.
- ALGORITHMS CAN BE EASILY CONVERTED FROM ONE CHIP TO A LARGER VERSION WHEN MORE SPACE IS NEEDED PART WAY THROUGH A PROGRAM.

MAY OPERATIONS REVIEW
COMPONENT DESIGN

EFFICIENCY OF BAR AREA

	LCD III-"C" CHIP	TMS 0500/TMS 0580, 0501
ROM SIZE	3K x 12 BIT (36,864 BITS)	2.5K X 13 BIT (33,280 BITS)
RAM SIZE	20 REGISTERS (1280 BITS)	13 REGISTERS (832 BITS)
BAR SIZE/CHIP	48K SQ. MILS.	TMS 0580 = 48K SQ. MILS. TMS 0501 = 55K SQ. MILS.
TOTAL BAR AREA	48K SQ. MILS	103K SQ. MILS.



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SYSTEM CONFIGURATIONS

- PRIMARY GOAL : SINGLE CHIP SYSTEM
  TP 0480

- LCD III PROCESSORS CAN BE TEAMED IN ANY DESIRED NUMBER, BUT BECOME INCREASINGLY DIFFICULT TO USE UNLESS EACH HAS A SPECIFIC TASK.
  EXAMPLE= PERIPHERALS

- EXPANSION DEVICES

  1. ROMS - MAX ≈ 35

     OR

  2. RAMS - MAX ≈ 35

     OR

  3. COMBINATION OF RAMS/ROMS ≈ 35

  4. MATRIX DISPLAY DRIVER — EXPANDABLE BY 8 DIGIT INCREMENTS TO ANY FORESEEABLE LENGTH

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PRODUCT X
DEFINITION REVIEW

PRODUCT OBJECTIVES

- TO PROVIDE UPGRADE LEADERSHIP PRODUCT TO REPLACE TI-59.
- EXPAND CONCEPTS OF PROBLEM SOLVING VIA CALCULATOR DEVICE.
- INCORPORATE:

  STATE-OF-THE-ART-TECHNOLOGIES

  SYSTEM DESIGN

  SYSTEM EXPANSION

- TO SIMPLIFY EASE OF USE AND PROVIDE MARKET EXPANSION AMONG PROFESSIONAL END USERS:

  TECHNICAL PROFESSIONALS

  NON-TECHNICAL PROFESSIONALS

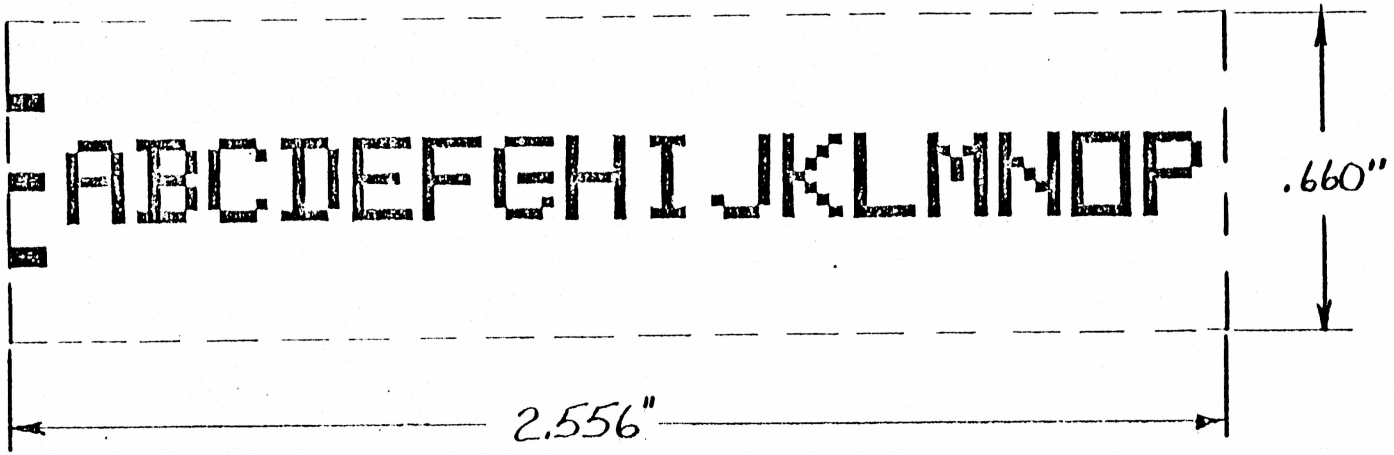
COMPONENT DESIGN

OPERATIONS REVIEW

PRODUCT X FEATURES

- EQUATION OPERATING SYSTEM (EOS)
- 16 CHARACTER 5 X 7 DOT MATRIX DISPLAY

  FULL ALPHANUMBERIC DISPLAY;EQUATION TRACE AND PROMPTING IN THE DISPLAY
- MORE FLEXIBLE USER MEMORY
  1. BASIC MEMORY IS 1000 PROGRAM STEPS OR 125 DATA REGISTERS WITH PARTITIONING BY THE USER
  2. SOLID STATE SOFTWARE APPROACH (CROM) HAS BEEN EXPANDED TO INCLUDE DROP-IN RAM (CRAM). CROMS AND CRAMS ARE INTERCHANGABLE AND TWO SLOTS ARE AVAILABLE ON THE CALCULATOR.
  3. BASIC MEMORY CAN BE EXPANDED TO 3000 PROGRAM STEPS OR 375 DATA REGISTERS
  4. CROMS WILL BE 15K PROGRAM STEPS
     - UP TO 99 PROGRAMS PER CROM
     - UP TO 10K STEPS PER PROGRAM
- EQUATION (EQN) MODE
  1. EQUATION CAN BE ENTERED WITHOUT EXECUTION
  2. DISPLAY WILL SCROLL WHEN FULL
  3. EQUATION MAY BE EDITED (BACKSTEP, INSERT,DELETE)
  4. EQUATION IS SAVED TO BE EXECUTED OR REPEATED WITH NEW DATA


ABCDEFGHIJKLMNOP
.660"
2.556"

COMPONENT DESIGN
OPERATIONS REVIEW
PRODUCT X APPROACH

GOAL: DEFINE AN OPERATING SYSTEM OR "LANGUAGE" FOR PRODUCT X THAT ALLOWS THE USER TO ENTER PROBLEMS AS THEY ARE NORMALLY WRITTEN

- EQUATION OPERATING SYSTEM (EOS)
- MORE POWERFUL THAN THE TI-59
- MUCH EASIER AND MORE OBVIOUS TO USE THAN TI-59
- UNARY AND BINARY OPERATIONS WILL BE ENTERED AS THEY ARE WRITTEN

  EXAMPLES: 2 X 3 =
  SIN 30 =

- AUTOMATIC VARIABLE ASSIGNMENT

  EXAMPLE: 30 => B 10 => C SIN B + C => A (A = 10.5)

- IMPLIED MULTIPLICATION

  EXAMPLES: SIN 2 π = CALCULATES THE SIN OF (2 X π)
  2A + B = CALCULATES (2 X A) + B

- INTEGER POWERS OF VARIABLES

  EXAMPLES: A5 MEANS THE VALUE STORED IN "A" RAISED TO THE 5TH POWER

COMPONENT DESIGN

OPERATIONS REVIEW

EXAMPLE: QUADRATIC EQUATION

PRODUCT X VS. HP 67 VS. TI-59 VS. SHARP 1300

FORMULA: $\frac{-B+\sqrt{B^2-4AC}}{2A}$

HP67: RCL B X^2 RCL A RCL C 4 X X - $\sqrt{X}$ RCL B - RCL A 2 X ÷

TI-59: (RCL 1 +/- + (X^2 - 4 X RCL 0 X RCL 2) $\sqrt{X}$) ÷ (2 X RCL 0) =

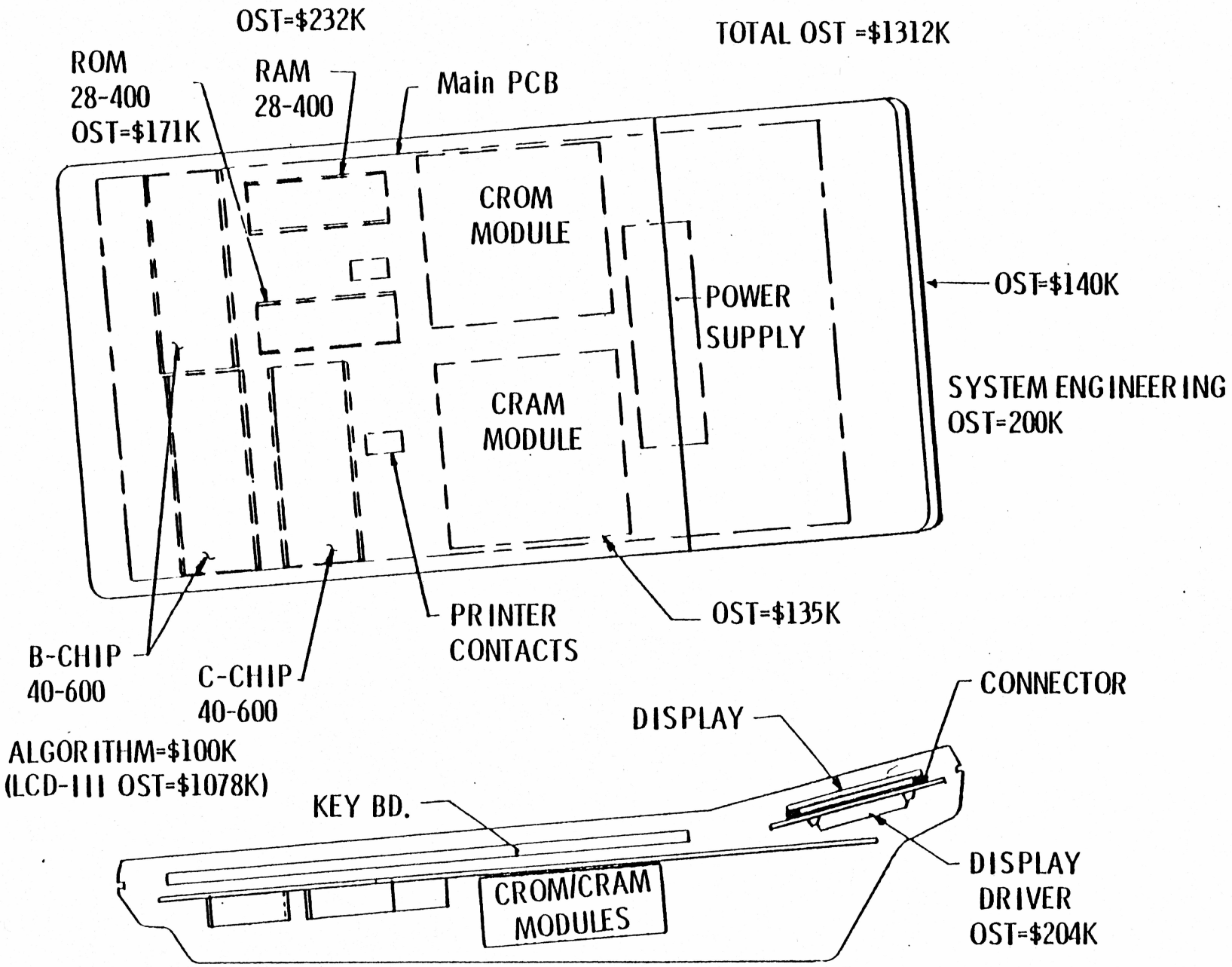
SHARP 1300: (-B + √(B * B - 4 * A * C)) ÷ (2 * A) =

PRODUCT X: (-B + √(B2 - 4AC)) ÷ 2A =

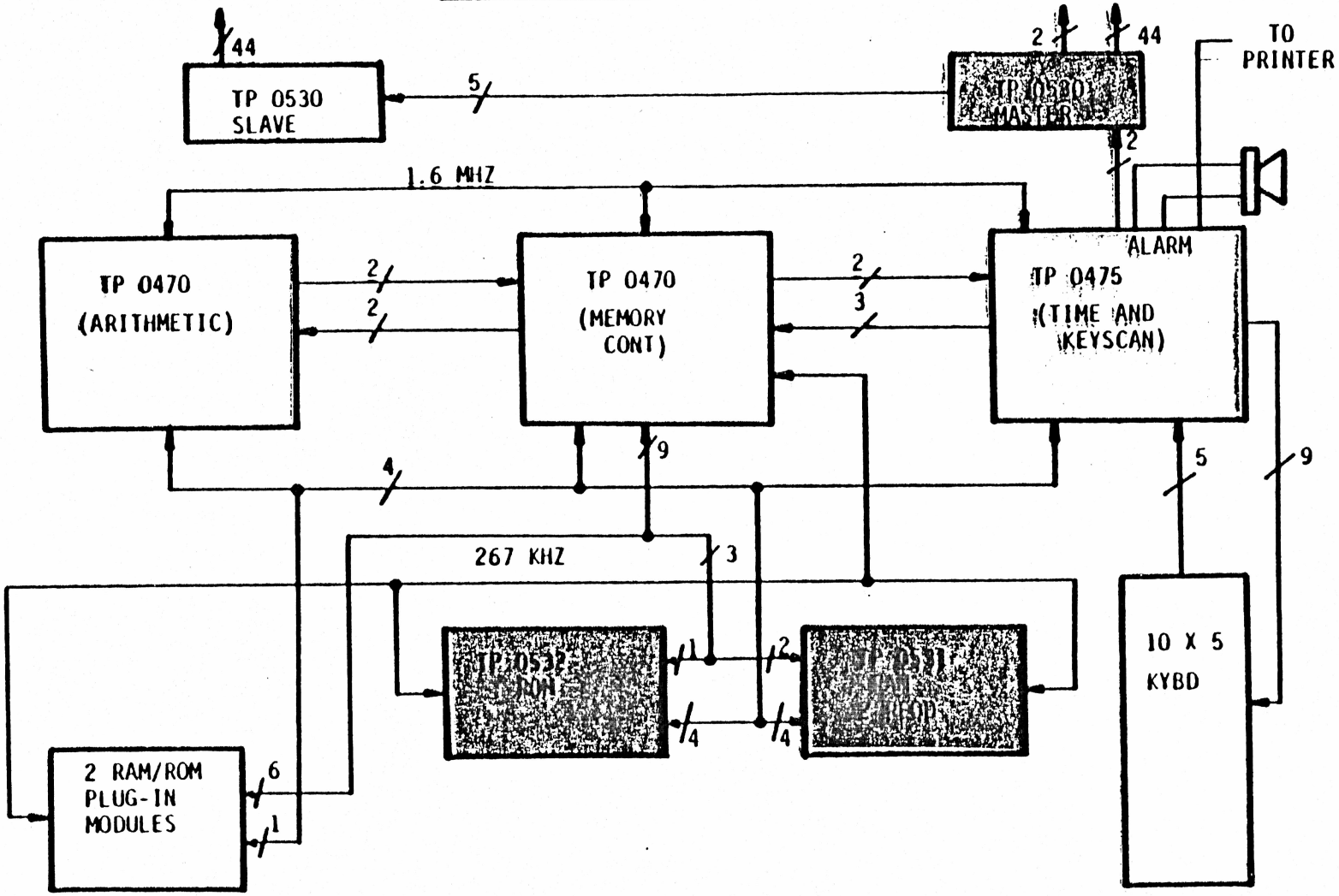
	HP 67	TI-59	SHARP 1300	PRODUCT X
NUMBER OF KEYSTROKES	22*	26	24	18

*20 + 2 2ND FUNCTION KEYS

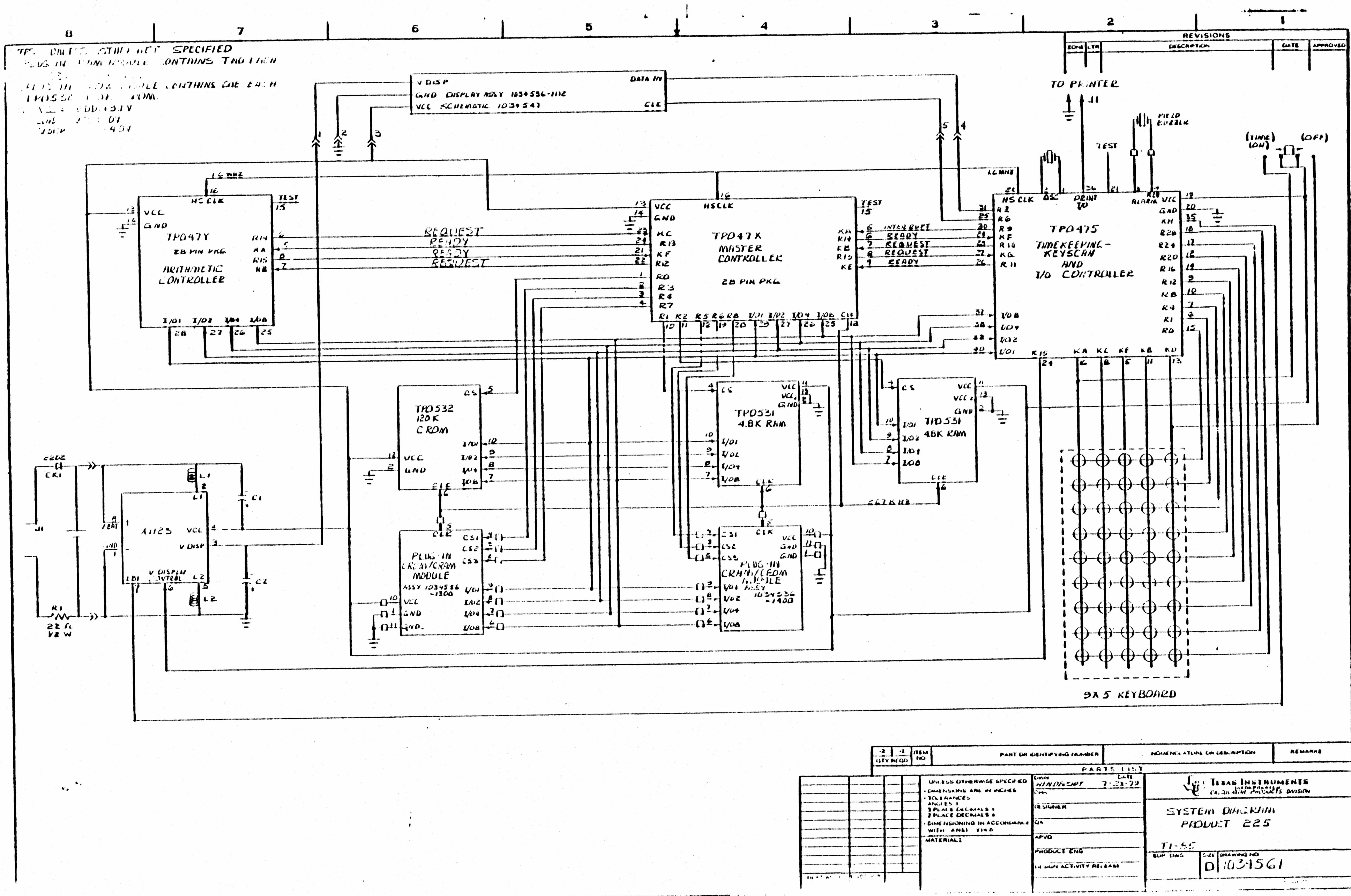
PRODUCT "X"


OST=$232K
TOTAL OST =$1312K
ROM
28-400
OST=$171K
RAM
28-400
Main PCB
CROM
MODULE
POWER
SUPPLY
OST=$140K
SYSTEM ENGINEERING
OST=200K
CRAM
MODULE
PRINTER
CONTACTS
OST=$135K
B-CHIP
40-600
C-CHIP
40-600
ALGORITHM=$100K
(LCD-III OST=$1078K)
CONNECTOR
DISPLAY
KEY BD.
CROM/CRAM
MODULES
DISPLAY
DRIVER
OST=$204K

U.S. CONSUMER GROUP
QUARTERLY FINANICAL REVIEW
COMPONENT DESIGN
PRODUCT X SYSTEM DIAGRAM



NOTE: EXTERNAL CHIP-INTERFACE THRU EITHER PLUG-IN MODULE


SPECIFIED
CONTAINS TWO EACH
TO PRINTER
PIEZO BUZZER
TEST
(TIME) (ON)
(OFF)
DISPLAY ASSY 1034536-1112
SCHEMATIC 1034541
V DISP
GND
VCC
DATA IN
CLK
TP0475
TIMEKEEPING-KEYSCAN AND I/O CONTROLLER
TP047X
MASTER CONTROLLER
28 PIN PKG
TP047Y
28 PIN PKG
ARITHMETIC CONTROLLER
REQUEST
READY
READY
REQUEST
INTERRUPT
TP0532
120K CROM
TP0531
4.8K RAM
PLUG-IN CROM/CROM MODULE
ASSY 1034536-1300
PLUG-IN CRAM/CROM MODULE
ASSY 1034536-1400
X1125
V DISPLAY CONTROL
9X5 KEYBOARD
REVISIONS
DESCRIPTION
DATE
APPROVED
PARTS LIST
PART OR IDENTIFYING NUMBER
NOMENCLATURE OR DESCRIPTION
REMARKS
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
DIMENSIONING IN ACCORDANCE WITH ANSI Y14.5
MATERIAL
7-21-72
TEXAS INSTRUMENTS
CALCULATOR PRODUCTS DIVISION
SYSTEM DIAGRAM
PRODUCT 225
TI-55
D 1034561

PRODUCT X REVIEW
COMPONENT DESIGN
PERIPHERAL INTERFACE

- PLUG-IN THROUGH CROM/CRAM SLOT (MEMORY EXPANSION)

  - 8 LINE CONNECTION
  - DATA RATE UP TO 266 K BITS/SECOND
  - MEMORY EXPANSION MODULE ACCEPTS UP TO 8 CROMS/CRAMS, CHIP SELECTS ARE GENERATED BY MEMORY CONTROLLER USING AN EXTERNAL MULTIPLEXER.

- SINGLE LINE PERIPHERAL CONNECTION

  - ONE REFERENCE LINE (GROUND) AND ONE SIGNAL LINE
  - PERIPHERALS ARE ON A COMMON BUS
  - A DEVICE IDENTIFIER PRECEDES COMMUNICATION
  - COMMUNICATION IS BETWEEN LCD PXT CHIP IN PRODUCT X AND AN EXTERNAL LCD III CHIP
  - INCLUDES PRINTER, CASSETTE, ETC.
  - DATA RATE UP TO 5K BITS/SECOND $\approx$ 40 LINES/SEC

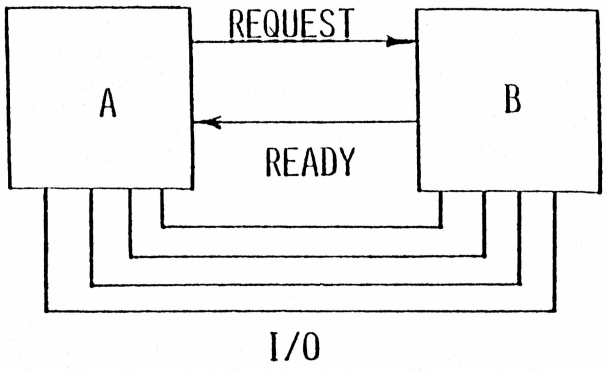
- CASSETTE ALTERNATIVE

  - SINCE KEYBOARD - I/O CONTROLLER NOW HAS 3K ROM AVAILABLE, THE CASSETTE INTERFACE COULD BE INCLUDED ON THIS CHIP AT NO ADDITIONAL COST.
  - THIS WOULD REQUIRE LEVEL BUFFERING AND THREE ADDITIONAL JACKS ON PRODUCT X. (MICROPHONE, EARPHONE, AND PAUSE JACKS)

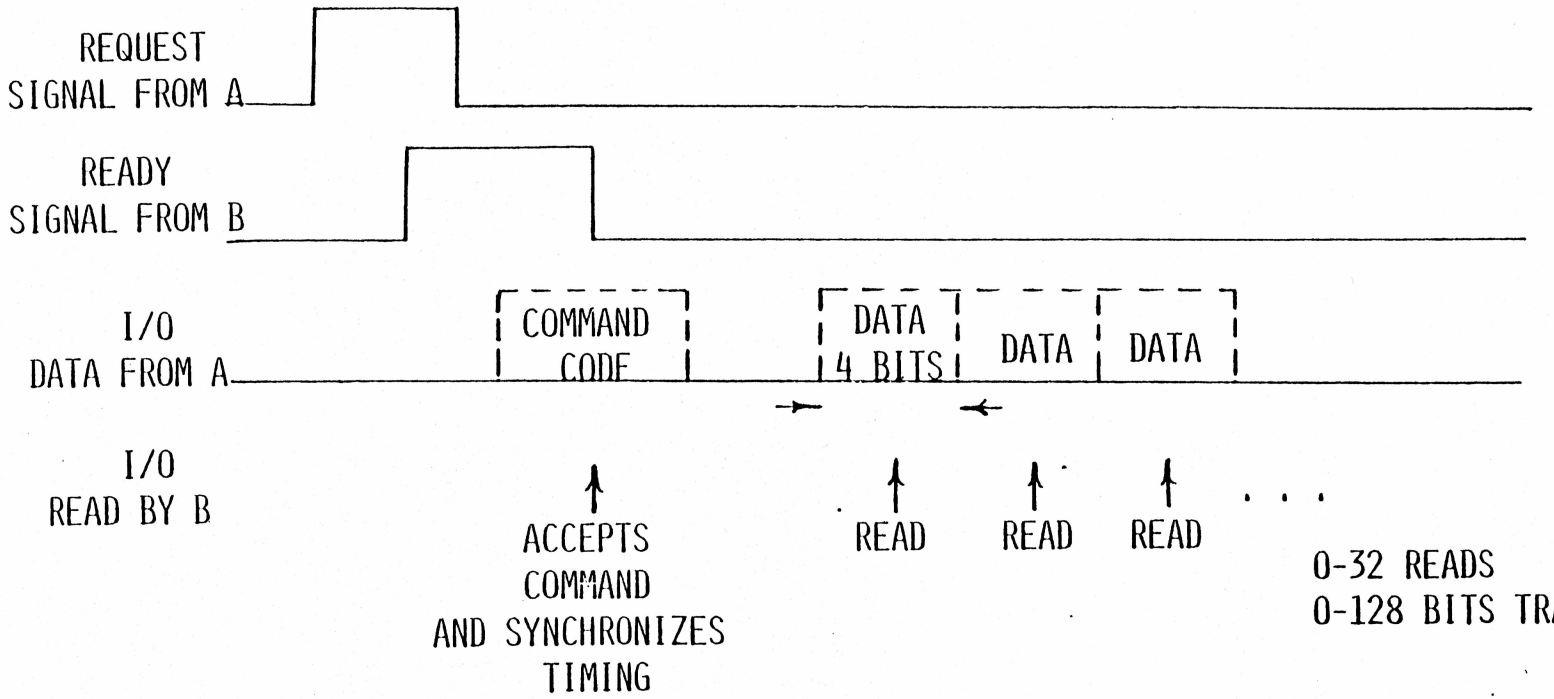
PRODUCT X REVIEW

COMMUNICATION TECHNIQUES

ON BOARD CHIP TO CHIP COMMUNICATION



A TO B COMMUNICATION



PRODUCT X ELECTRICAL DESIGN REVIEW

PERIPHERAL COMMUNICATION

- PRODUCT X CALCULATOR IS NORMALLY MASTER
  - WILL MONITOR INCOMING TRANSMISSIONS AND ALLOW A DEVICE TO BECOME MASTER IF CALCULATOR IS IDLE
- EACH PERIPHERAL AND THE CALCULATOR HAS A DEVICE CODE
  - COMMUNICATION IS BETWEEN:
    1. CALCULATOR AND A PERIPHERAL
    2. TWO PERIPHERALS
    3. TWO CALCULATORS
- CALCULATOR HAS OP CODES TO SEND AND RECEIVE ON PERIPHERAL I/O AND THESE ARE PROGRAMMABLE
- COMMUNICATION STRING CONTAINS:
  1. START CODE
  2. RECEIVING DEVICE CODE
  3. SENDING DEVICE CODE
  4. COMMAND CODE
  5. 128 BITS OF DATA
  6. ERROR DETECTION/CORRECTION ?

PERIPHERAL COMMUNICATION (CONTINUED)

- AN OP CODE FOR SLOW SPEED TRANSMISSION WILL BE AVAILABLE FOR COMMUNICATION TO SLOWER PROCESSORS SUCH AS TPO455. DATA RATE ≈ 10 LINES/SEC.

- BIT TRANSMISSION WILL BE RATIO DETECTION FOR GOOD NOISE PROTECTION AND FREQUENCY TOLERANCE

ONE ZERO

- DOUBLE DETECTION OF TRANSITIONS WILL BE USED TO PROVIDE ACCURATE BIT CLOCKING.

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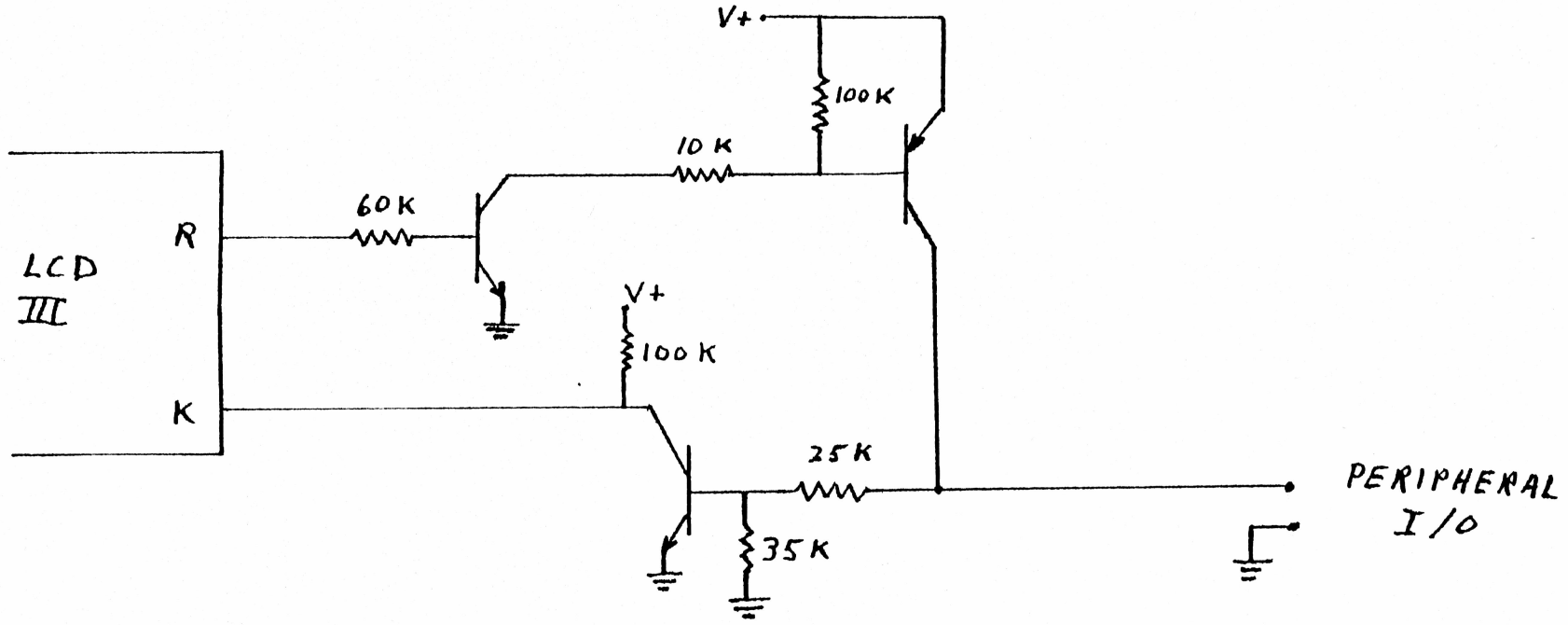

3.1v Max. LOGIC 1

2.4v Min. LOGIC 1

1.2v TRANSITION VOLTAGE

0v LOGIC 0

MINIMUM NOISE MARGIN FOR LOGIC 1 OR 0 = 1.2 v

CALCULATOR POWER SUPPLY MUST PROVIDE ~ 2 MA TO DRIVE 16 PERIPHERALS

REQUIRES ~ .5 MA FOR 1 PERIPHERAL

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